Listing of Claims

Claims 1 – 2 (canceled)

3. (previously presented): A method of forming a capacitor in an integrated circuit comprising:

(a) forming a lower electrode layer on a semiconductor body;

(b) forming a dielectric layer over a portion of said lower electrode layer;

(c) forming an upper electrode layer over a portion of said dielectric layer;

(d) removing a portion of said upper electrode layer to expose a portion of said dielectric layer, thereby forming an upper electrode with a lateral boundary, wherein a portion of said dielectric layer is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary of said upper electrode and between said lower electrode layer and said upper electrode;

(e) subsequently removing a portion of said exposed portion of said dielectric layer to expose a portion of said lower electrode layer, wherein a portion of said dielectric layer is removed from said inter-electrode region;

(f) subsequently forming a conformal insulating layer over a portion of said exposed portion of said lower electrode layer proximate to said portion of said dielectric layer disposed in said inter-electrode region, whereby a portion of conformal insulating layer is formed in said inter-electrode region; and

(g) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal insulating layer.

4. (previously presented): The method of claim 3, wherein said conformal insulating layer has a thickness ranging from 20 angstroms to 70 angstroms.

5. (previously presented): The method of claim 3, wherein said conformal insulating layer is an oxide layer formed in a thermal process.

6. (previously presented): The method of claim 5, wherein said thermal process is a rapid thermal oxidation (RTO) performed for a length of time ranging from 10 to 60 seconds and at a temperature ranging from 850°C to 1050°C.

7. (previously presented): The method of claim 3, wherein said conformal insulating layer is formed by deposition.

8. (original): The method of claim 3, wherein said ARL is an anti-reflective coating.

9. (original): The method of claim 3, wherein said ARL is titanium nitride.

10. (original): The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. (previously presented): The method of claim 10, wherein said plasma enhanced chemical vapor deposition anti-reflective layer (PEARL) has a thickness ranging from 300 angstroms to 400 angstroms.

Claims 12 – 35 (canceled)

36. (previously presented): A method of forming an integrated circuit comprising:

(a) forming a conductive layer on a semiconductor body;

(b) forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer, wherein said top electrode has a lateral boundary; and

a dielectric layer between said top electrode and said conductive layer;

(c) forming a conformal insulating layer over said capacitor structure and a portion of said conductive layer proximate to said capacitor structure, wherein a portion of said conformal insulating layer is formed in an inter-electrode region

within said lateral boundary of said top electrode and between said top electrode and said conductive layer;

(d) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal layer;

(e) forming a patterned mask over said anti-reflective layer (ARL); and

(f) etching said conductive layer using said patterned mask.

37. (previously presented): The method of claim 36, wherein said conformal insulating layer has a thickness ranging from 20 angstroms to 70 angstroms.

38. (previously presented): The method of claim 36, wherein said conformal insulating layer is an oxide layer formed in a thermal process.

39. (previously presented): The method of claim 36, wherein said conductive layer is additionally used to form a gate of one or more transistors formed on said integrated circuit.

Claims 40 – 71 (canceled)

72. (previously presented): The method of claim 3, further comprising:

(h) forming a photoresist mask over a portion of said anti-reflective layer (ARL); and

(i) irradiating said photoresist mask with radiation that penetrates said photoresist mask, wherein said anti-reflective layer reduces a reflection of said radiation by 70% or more.

73. (previously presented): The method of claim 72, wherein the anti-reflective layer reduces said reflection of said radiation by 70% to 85%.

74. (previously presented): The method of claim 3, wherein said anti-reflective layer is a Si_xON_y film.

Claims 75 – 101 (canceled)

102. (previously presented): The method of claim 3, wherein said subsequently removing a portion of said exposed portion of said dielectric layer in step (e) is performed using isotropic wet etching.

103. (previously presented): A method comprising:

(a) forming a lower electrode layer upon an underlying layer of a semiconductor device;

(b) forming a capacitor dielectric layer;

(c) forming an upper electrode layer, wherein said capacitor dielectric layer is disposed in an inter-electrode region between said lower electrode layer and said upper electrode layer;

(d) removing a portion of said upper electrode layer such that an upper electrode is formed having an edge;

(e) removing a portion of said dielectric layer such that an exposed portion of said lower electrode layer is formed and such that an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting;

(f) providing a conformal insulating layer over said upper electrode and over said exposed portion of said lower electrode layer such that said undercutting is filled in by said conformal insulating layer; and

(g) providing a anti-reflective layer over said conformal insulating layer.

104. (previously presented): The method of claim 103, wherein the forming in step (b) is performed by depositing said capacitor dielectric layer to a thickness ranging from 300 angstroms to 800 angstroms.

105. (previously presented): The method of claim 103, wherein said underlying layer electrically isolates said lower electrode layer.

106. (previously presented): The method of claim 103, wherein the providing the conformal insulating layer in step (f) is performed using a rapid thermal oxidation (RTO) process to grow a layer of silicon oxide to a thickness ranging from 20 angstroms to 100 angstroms.

107. (previously presented): A method comprising:

(a) forming a lower electrode layer upon an underlying layer of a semiconductor device;

(b) forming a capacitor dielectric layer;

(c) forming an upper electrode layer, wherein said capacitor dielectric layer is disposed in an inter-electrode region between said lower electrode layer and said upper electrode layer;

(d) removing a portion of said upper electrode layer such that an upper electrode is formed;

(e) removing a portion of said dielectric layer using anisotropic etching such that an undercutting is formed underneath said upper electrode, wherein said dielectric layer is absent from said undercutting;

(f) providing a conformal insulating layer over said upper electrode such that said undercutting is filled in by said conformal insulating layer; and

(g) providing a anti-reflective layer over said conformal insulating layer.

108. (previously presented): The method of claim 107, wherein said anisotropic etching is a buffered oxide etch (BOE).

109. (withdrawn): A device comprising:

a lower electrode layer disposed on an underlying layer of a semiconductor substrate;

a capacitor dielectric disposed on said lower electrode layer;

an upper electrode disposed on said capacitor dielectric, wherein said upper electrode has a lateral boundary, wherein said capacitor dielectric is disposed

within an inter-electrode region, said inter-electrode region disposed within said lateral boundary between said lower electrode layer and said upper electrode layer, and wherein an exposed portion of said lower electrode layer lies outside said lateral boundary;

a conformal layer of an insulating material disposed over said upper electrode and over said exposed portion of said lower electrode layer;

an undercutting in said inter-electrode region, wherein said capacitor dielectric is absent from said undercutting and said undercutting is filled by said insulating material; and

an anti-reflective layer disposed over said conformal layer of said insulating material.

110. (withdrawn): The device of claim 109, wherein said anti-reflective layer is titanium nitride.

111. (withdrawn): The device of claim 109, wherein said anti-reflective layer is a plasma enhanced anti-reflective layer (PEARL).

112. (withdrawn): The device of claim 109, wherein said lower electrode layer is polysilicon.

113. (withdrawn): A device comprising:

a lower electrode layer disposed on an underlying layer of a semiconductor substrate;

a capacitor dielectric disposed on said lower electrode layer;

an upper electrode disposed on said capacitor dielectric, wherein said upper electrode has a lateral boundary, wherein said capacitor dielectric is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary and between said lower electrode layer and said upper electrode layer, and wherein an exposed portion of said lower electrode layer lies outside said lateral boundary;

an anti-reflective layer disposed over said upper electrode and over said exposed portion of said lower electrode layer; and

means for preventing an electrical connection through said anti-reflective layer from said upper electrode to said lower electrode layer, wherein said means is at least partially disposed within said inter-electrode region.

114. (withdrawn): The device of claim 113, wherein said anti-reflective layer is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).